Fig. 1

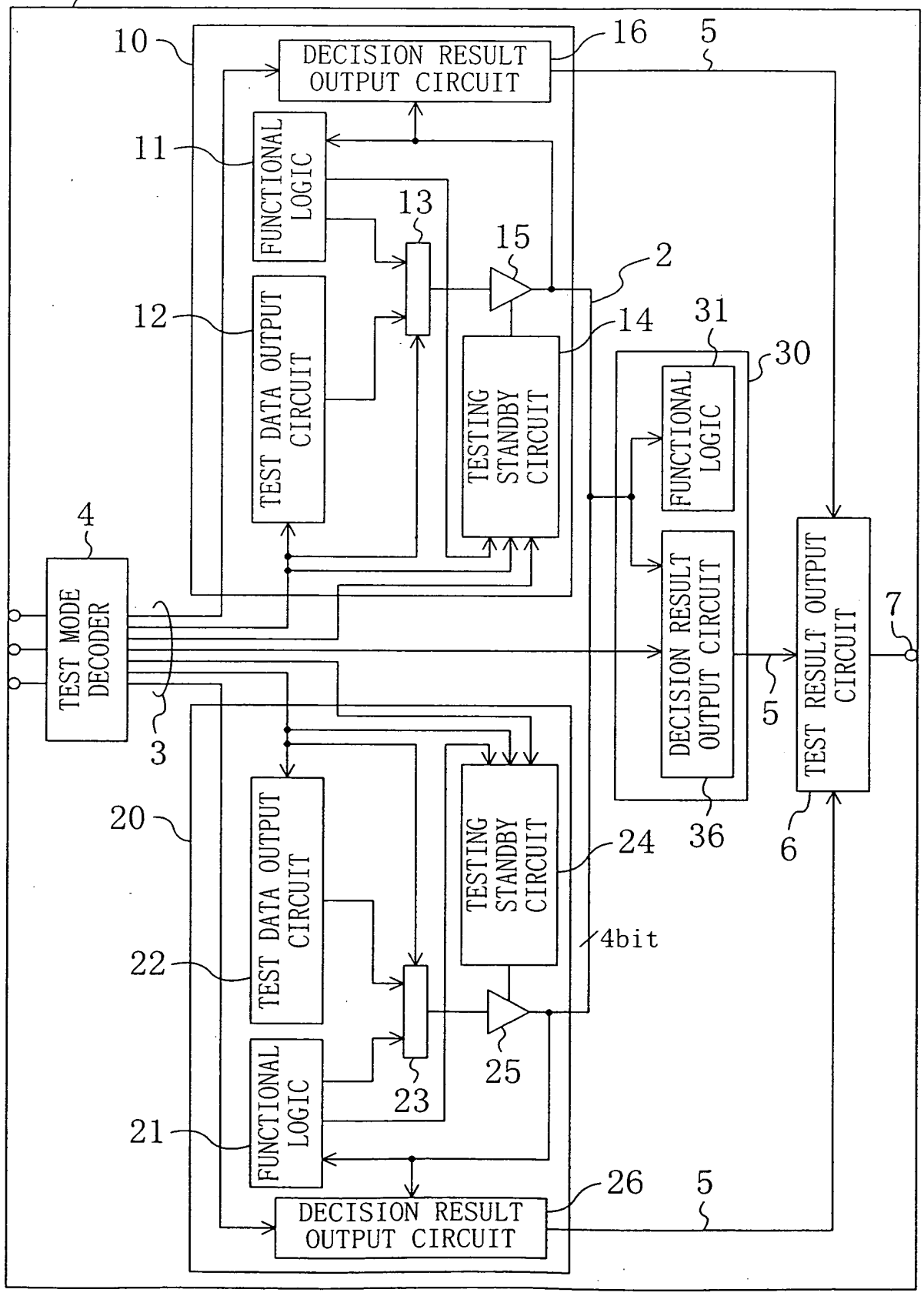
1
10
DECISION RESULT OUTPUT CIRCUIT
16
5
11
FUNCTIONAL LOGIC
13
15
2
12
TEST DATA OUTPUT CIRCUIT
14
TESTING STANDBY CIRCUIT
31
30
FUNCTIONAL LOGIC
4
TEST MODE DECODER
DECISION RESULT OUTPUT CIRCUIT
TEST RESULT OUTPUT CIRCUIT
7
3
5
20
TEST DATA OUTPUT CIRCUIT
TESTING STANDBY CIRCUIT
24
36
6
4bit
22
23
25
21
FUNCTIONAL LOGIC
26
5
DECISION RESULT OUTPUT CIRCUIT

Fig. 2

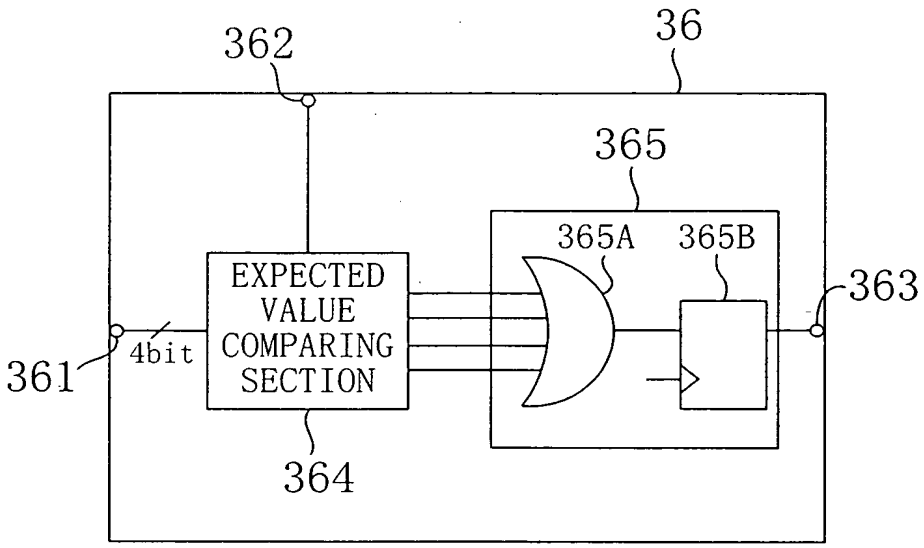
362
36
365
365A
365B
363
EXPECTED VALUE COMPARING SECTION
4bit
361
364

Fig. 3

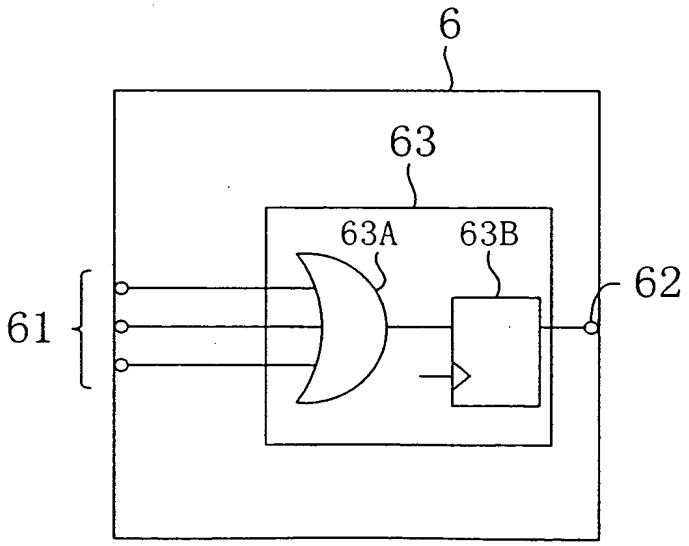
6
63
63A
63B
62
61

Fig. 4

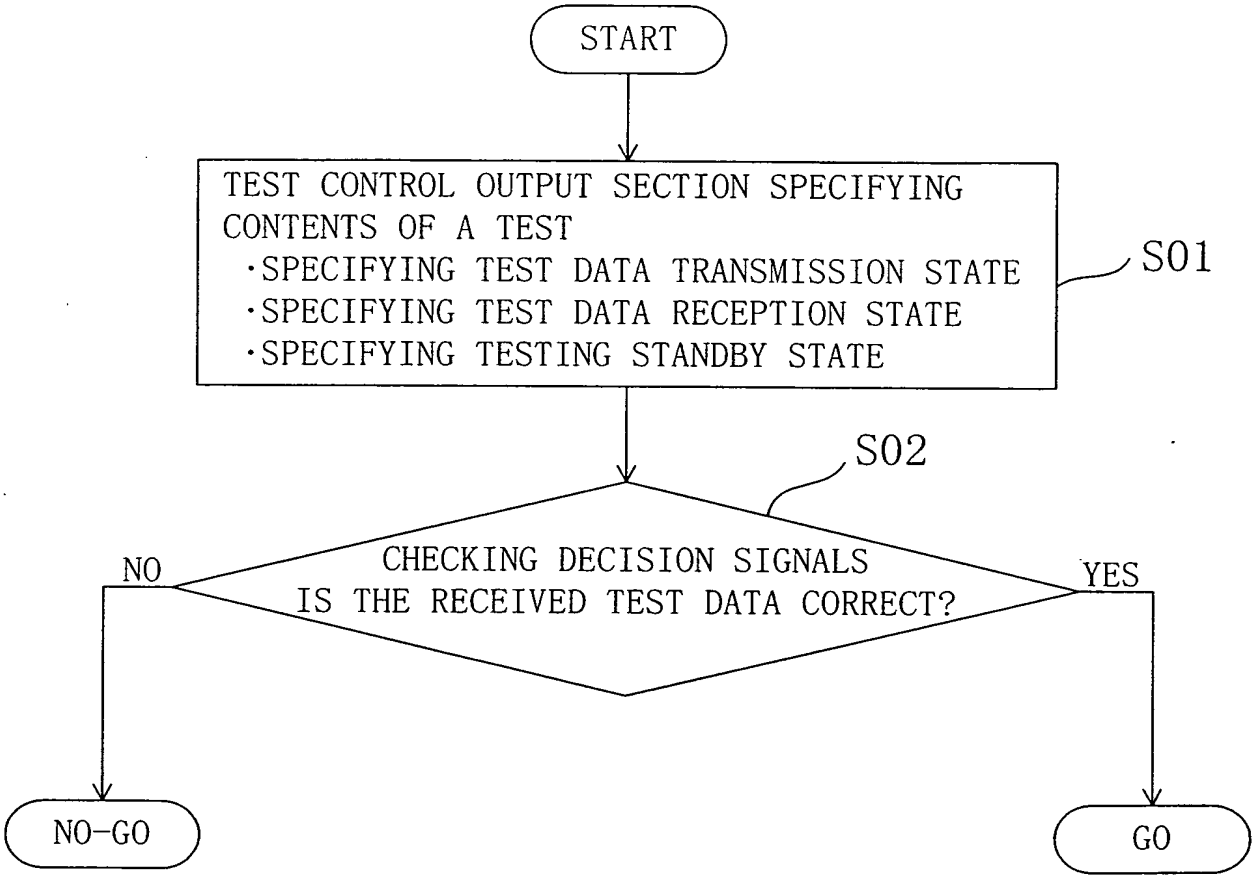
START
TEST CONTROL OUTPUT SECTION SPECIFYING CONTENTS OF A TEST
·SPECIFYING TEST DATA TRANSMISSION STATE
·SPECIFYING TEST DATA RECEPTION STATE
·SPECIFYING TESTING STANDBY STATE
S01
S02
CHECKING DECISION SIGNALS
IS THE RECEIVED TEST DATA CORRECT?
NO
YES
NO-GO
GO

Fig. 5

TIME / TEST DATA	t 1	t 2
BIT 0	1	0
BIT 1	1	0
BIT 2	1	0
BIT 3	1	0

Fig. 6

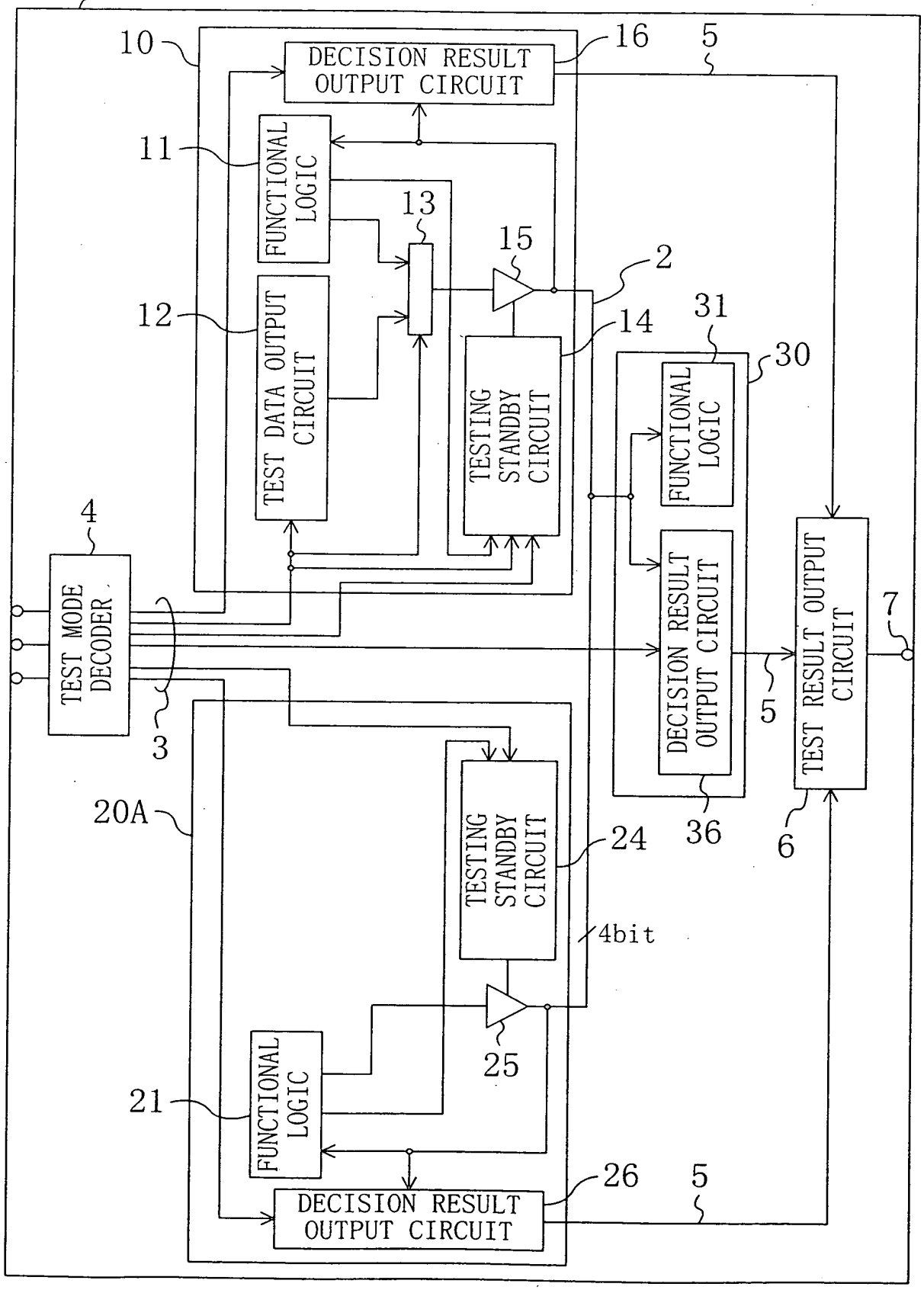
1
10
DECISION RESULT OUTPUT CIRCUIT
16
5
11
FUNCTIONAL LOGIC
13
15
2
12
TEST DATA OUTPUT CIRCUIT
14
TESTING STANDBY CIRCUIT
31
30
FUNCTIONAL LOGIC
4
TEST MODE DECODER
DECISION RESULT OUTPUT CIRCUIT
TEST RESULT OUTPUT CIRCUIT
7
3
5
20A
TESTING STANDBY CIRCUIT
24
36
6
4bit
25
21
FUNCTIONAL LOGIC
26
5
DECISION RESULT OUTPUT CIRCUIT

Fig. 7

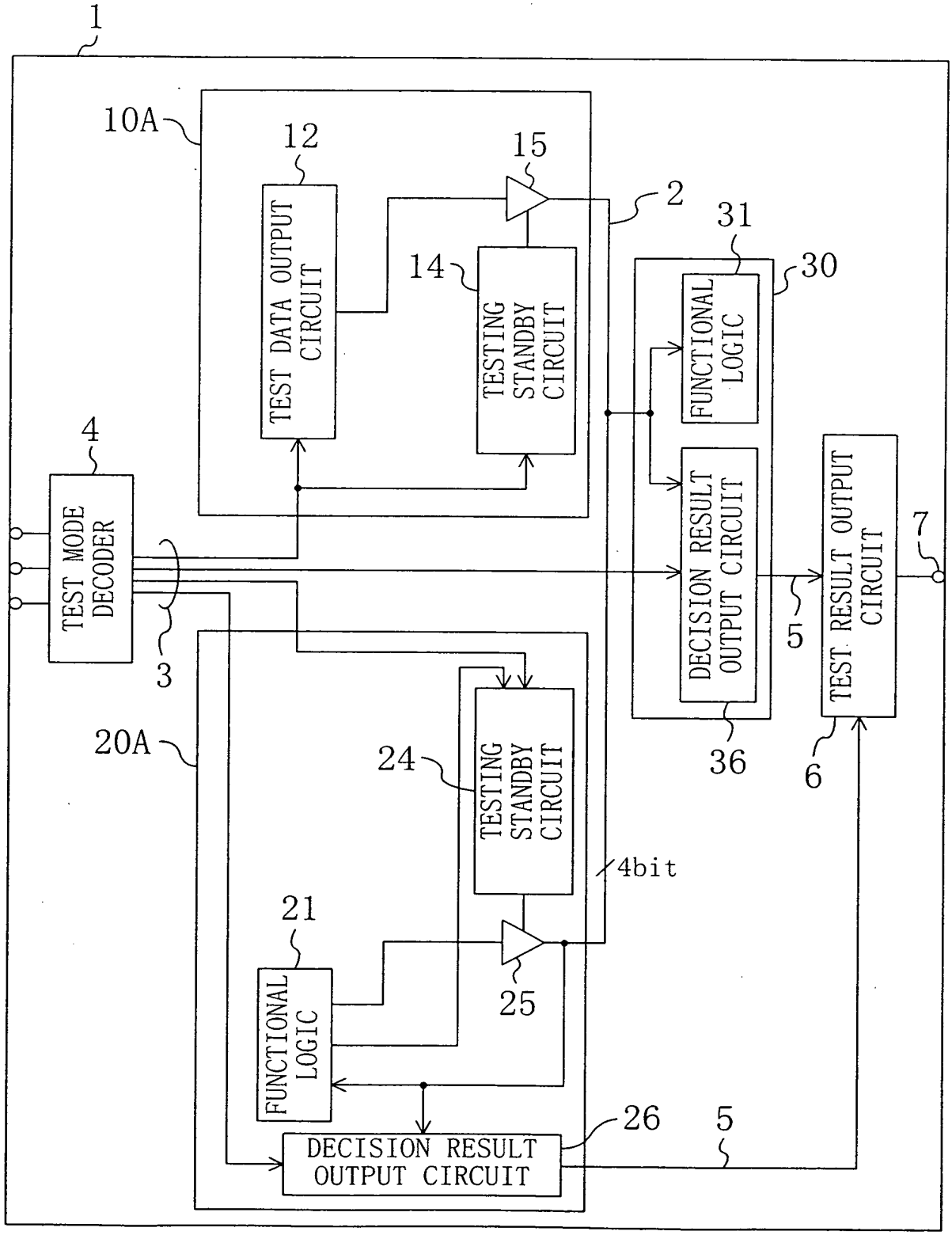
1
10A
12
TEST DATA OUTPUT CIRCUIT
15
2
14
TESTING STANDBY CIRCUIT
31
30
FUNCTIONAL LOGIC
4
TEST MODE DECODER
DECISION RESULT OUTPUT CIRCUIT
TEST RESULT OUTPUT CIRCUIT
7
5
3
20A
24
TESTING STANDBY CIRCUIT
36
6
4bit
21
25
FUNCTIONAL LOGIC
26
5
DECISION RESULT OUTPUT CIRCUIT

Fig. 8

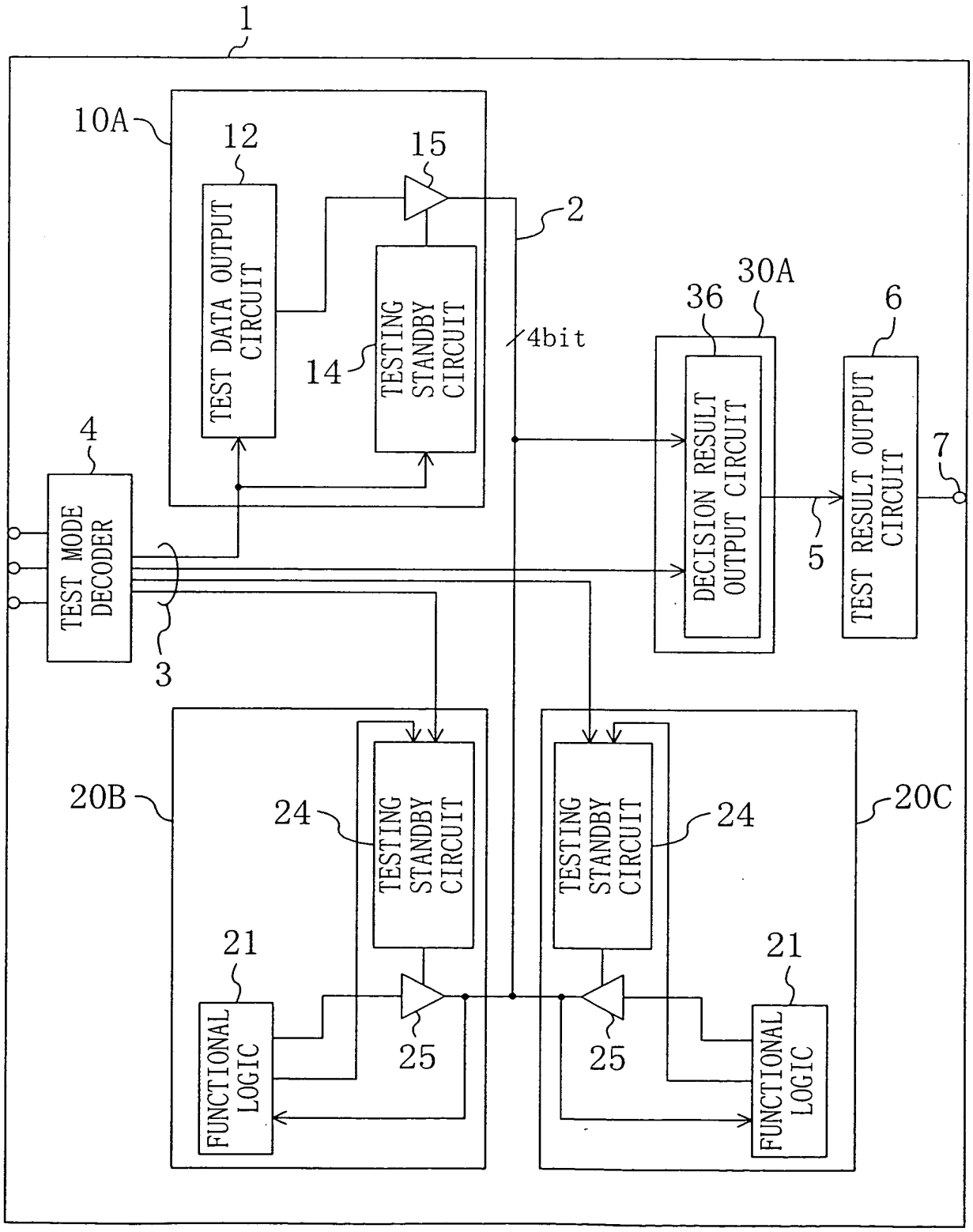
1
10A
12
TEST DATA OUTPUT CIRCUIT
15
2
14
TESTING STANDBY CIRCUIT
4bit
30A
36
DECISION RESULT OUTPUT CIRCUIT
6
TEST RESULT OUTPUT CIRCUIT
7
5
4
TEST MODE DECODER
3
20B
24
TESTING STANDBY CIRCUIT
21
FUNCTIONAL LOGIC
25
20C
24
TESTING STANDBY CIRCUIT
21
FUNCTIONAL LOGIC
25

Fig. 9

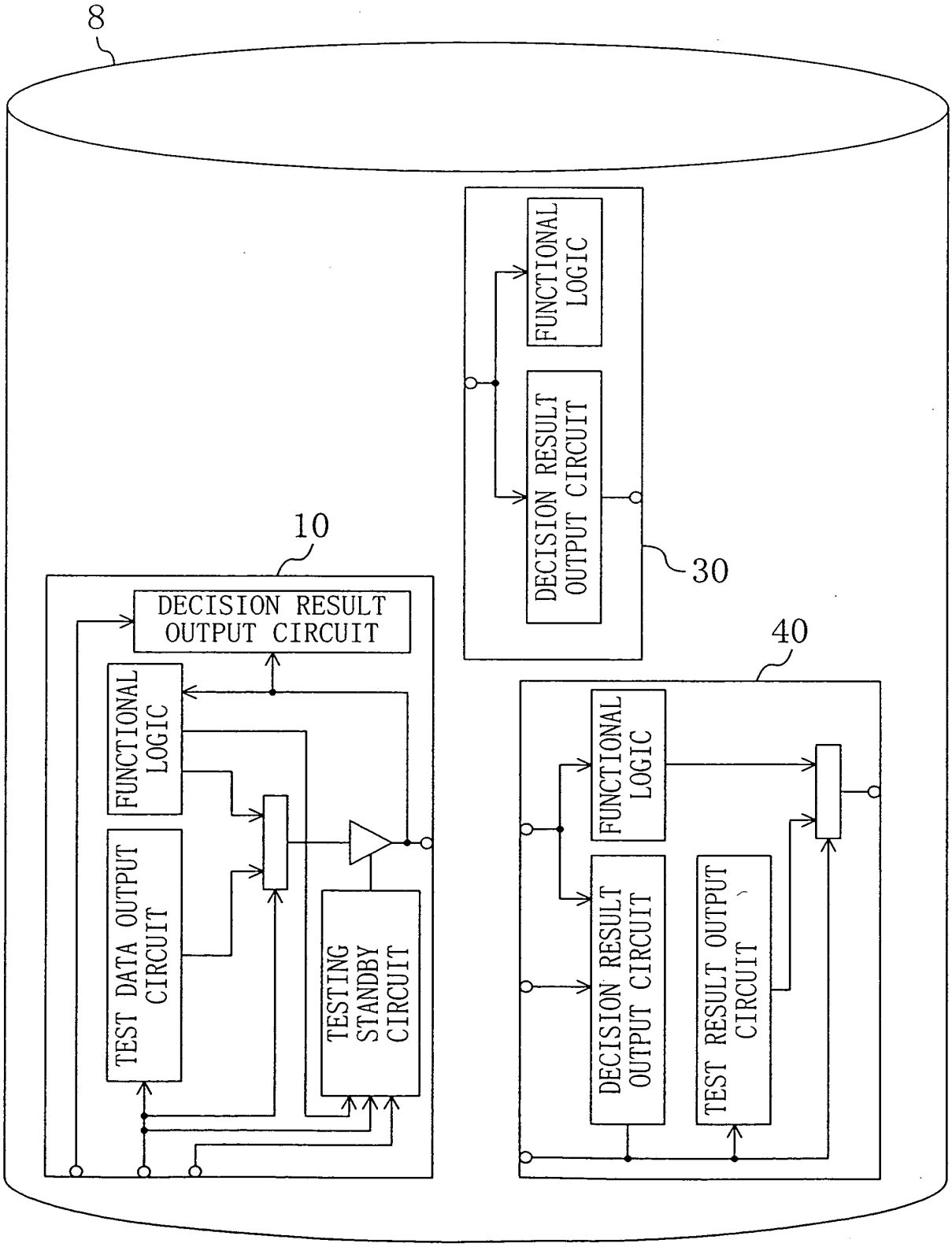
8
FUNCTIONAL LOGIC
DECISION RESULT OUTPUT CIRCUIT
30
10
DECISION RESULT OUTPUT CIRCUIT
FUNCTIONAL LOGIC
TEST DATA OUTPUT CIRCUIT
TESTING STANDBY CIRCUIT
40
FUNCTIONAL LOGIC
DECISION RESULT OUTPUT CIRCUIT
TEST RESULT OUTPUT CIRCUIT

Fig. 10

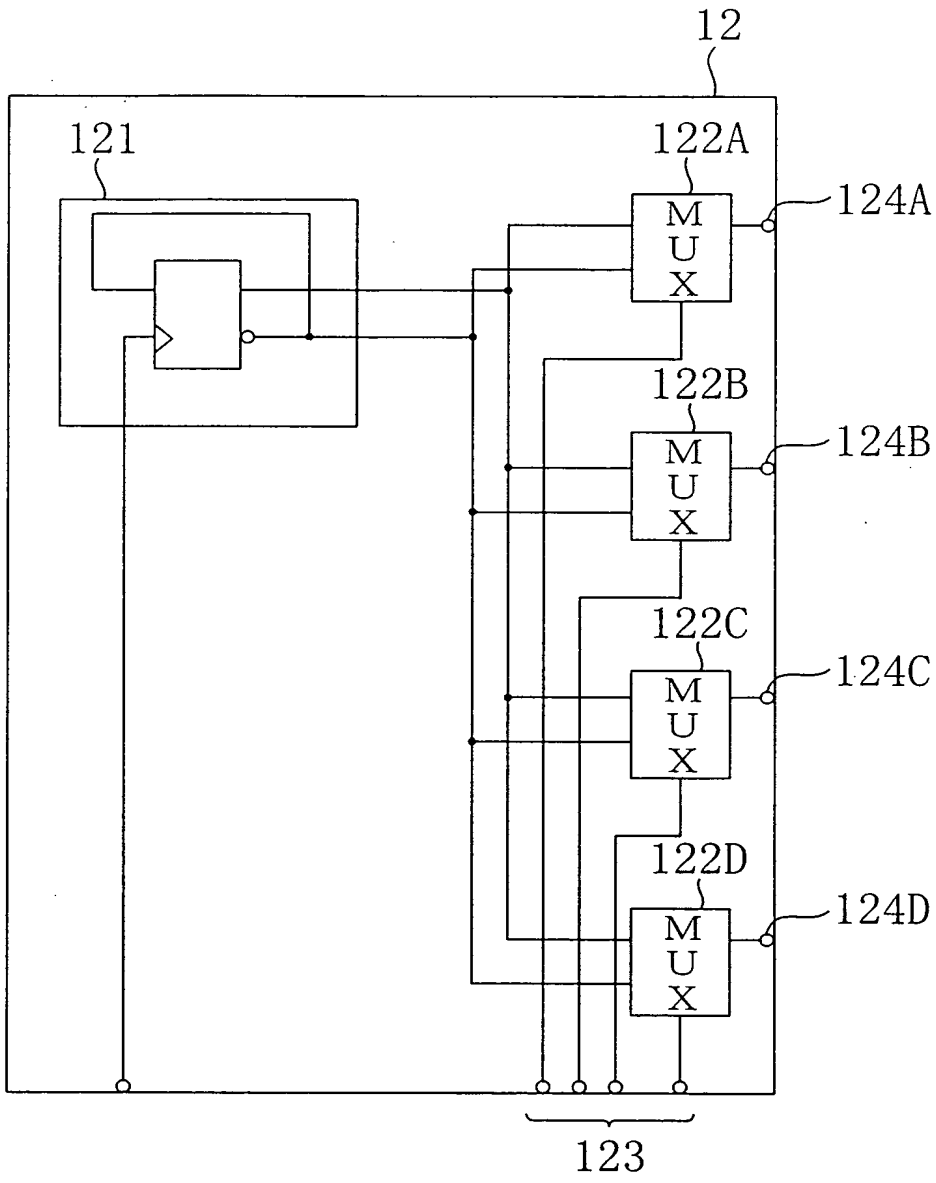
12
121
122A
124A
M
U
X
122B
124B
M
U
X
122C
124C
M
U
X
122D
124D
M
U
X
123

Fig. 11

TIME / TEST DATA	t 1	t 2
BIT 0	1	0
BIT 1	0	1
BIT 2	1	0
BIT 3	0	1

Fig. 12

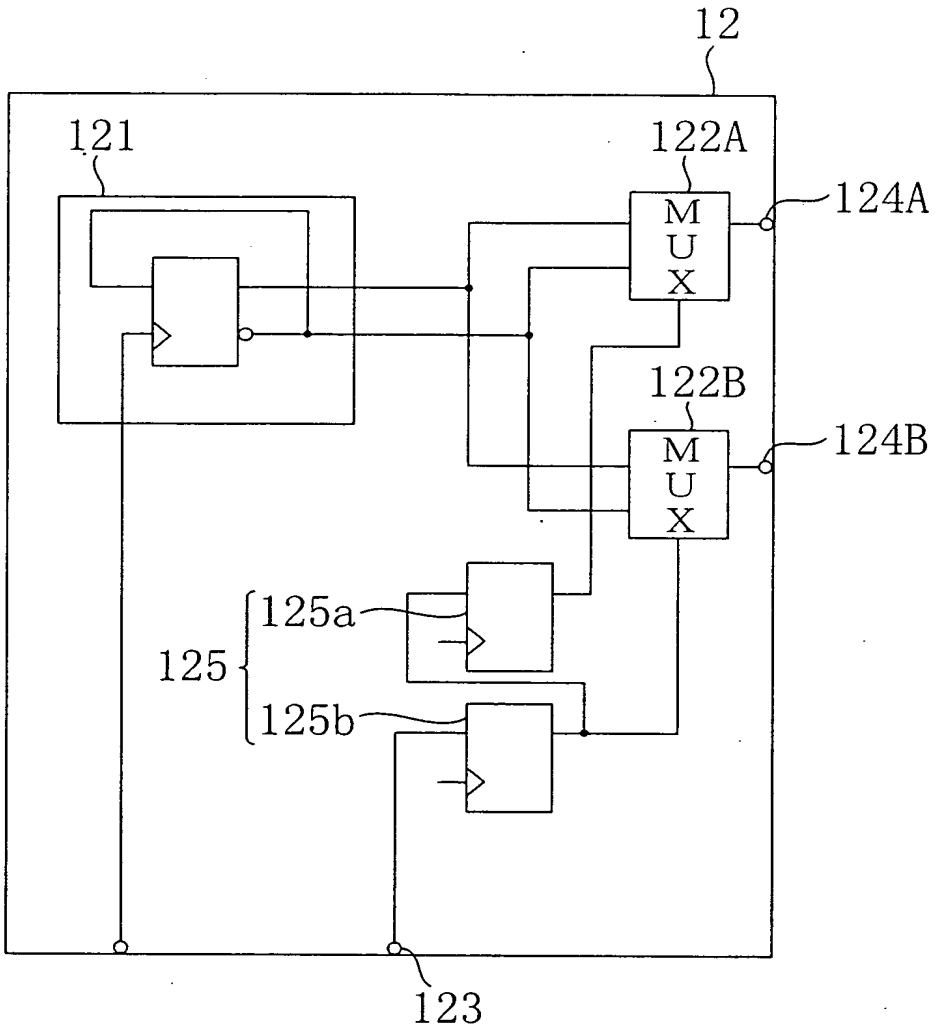

Fig. 13

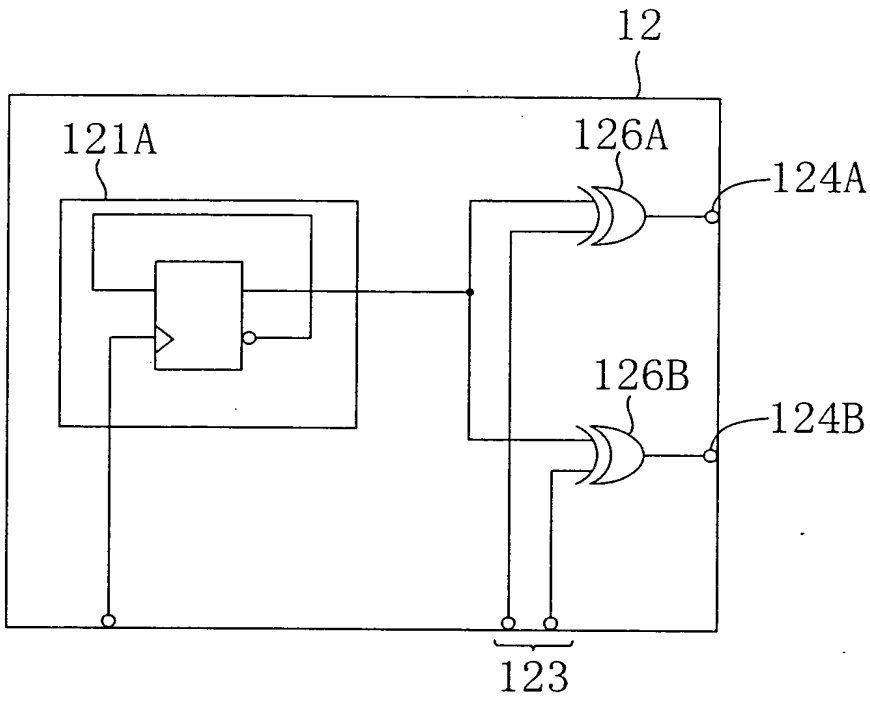

Fig. 14

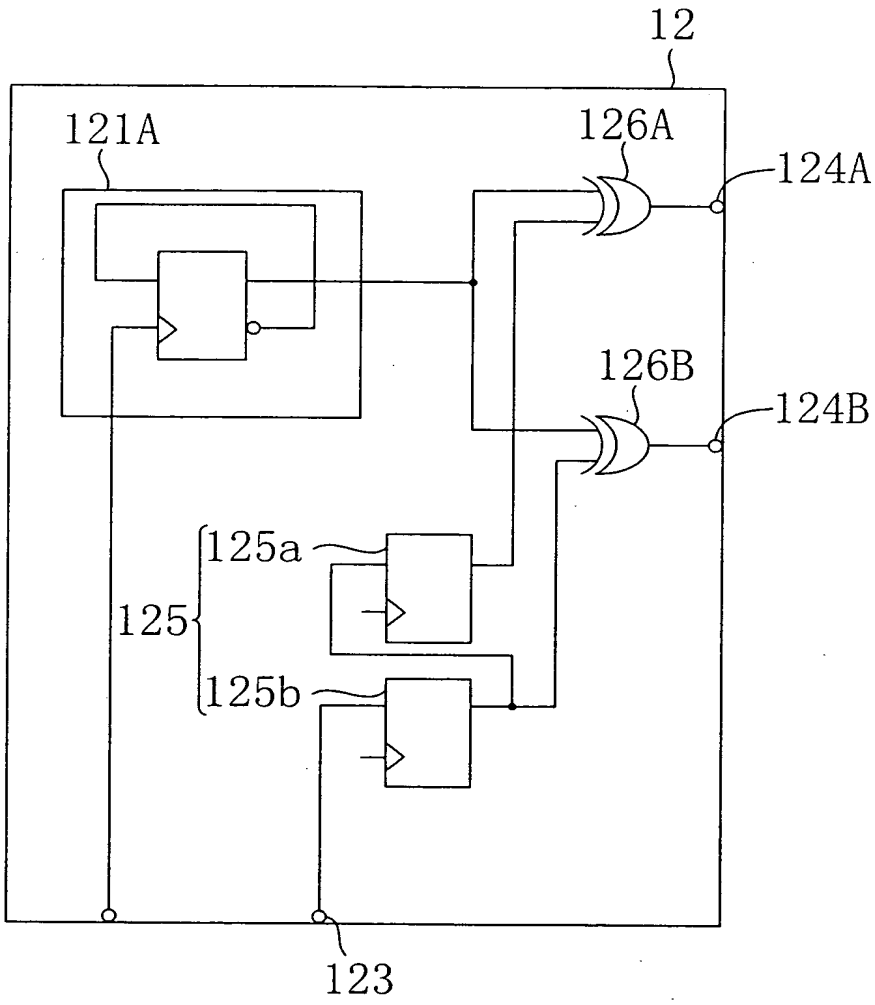

Fig. 15(a)

	t 1	t 2	t 3	t 4
BIT 0	0	1	0	1
BIT 1	0	1	0	1
BIT 2	0	1	0	1
BIT 3	0	1	0	1
BIT 4	1	0	1	0
BIT 5	1	0	1	0
BIT 6	1	0	1	0
BIT 7	1	0	1	0

GROUP

Fig. 15(b)

	t 5	t 6	t 7	t 8
BIT 0	0	1	0	1
BIT 1	0	1	0	1
BIT 2	1	0	1	0
BIT 3	1	0	1	0
BIT 4	0	1	0	1
BIT 5	0	1	0	1
BIT 6	1	0	1	0
BIT 7	1	0	1	0

GROUP

Fig. 15(c)

	t 9	t 10	t 11	t 12
BIT 0	0	1	0	1
BIT 1	1	0	1	0
BIT 2	0	1	0	1
BIT 3	1	0	1	0
BIT 4	0	1	0	1
BIT 5	1	0	1	0
BIT 6	0	1	0	1
BIT 7	1	0	1	0

GROUP

Fig. 16

TIME / TEST DATA	t 1	t 2	t 3
BIT 0	0	1	0
BIT 1	0	1	0
BIT 2	0	1	0
BIT 3	0	1	0

Fig. 17(a)

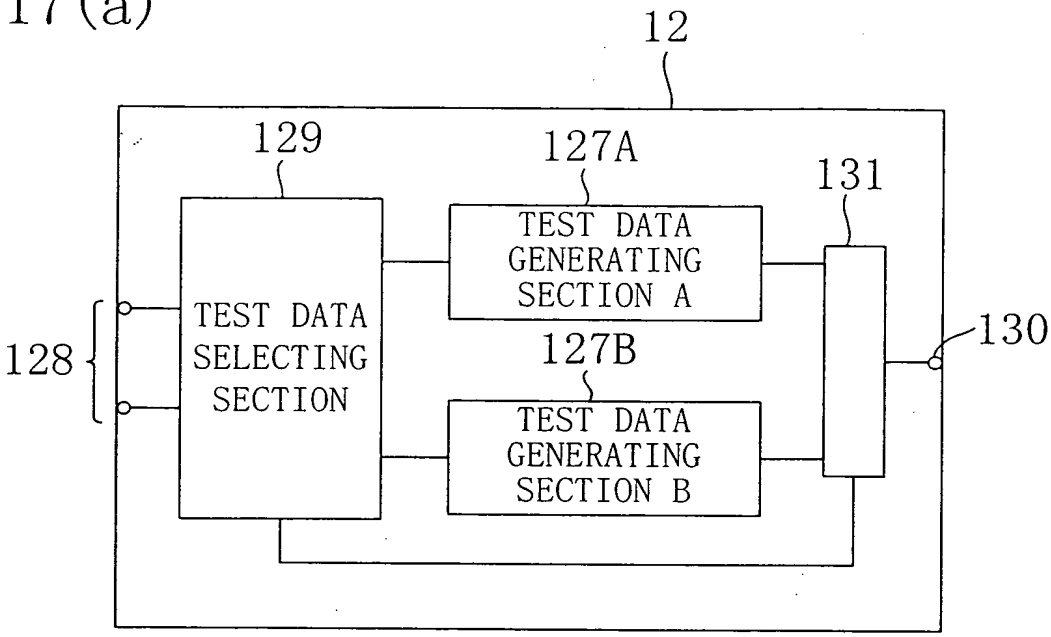

Fig. 17(b)

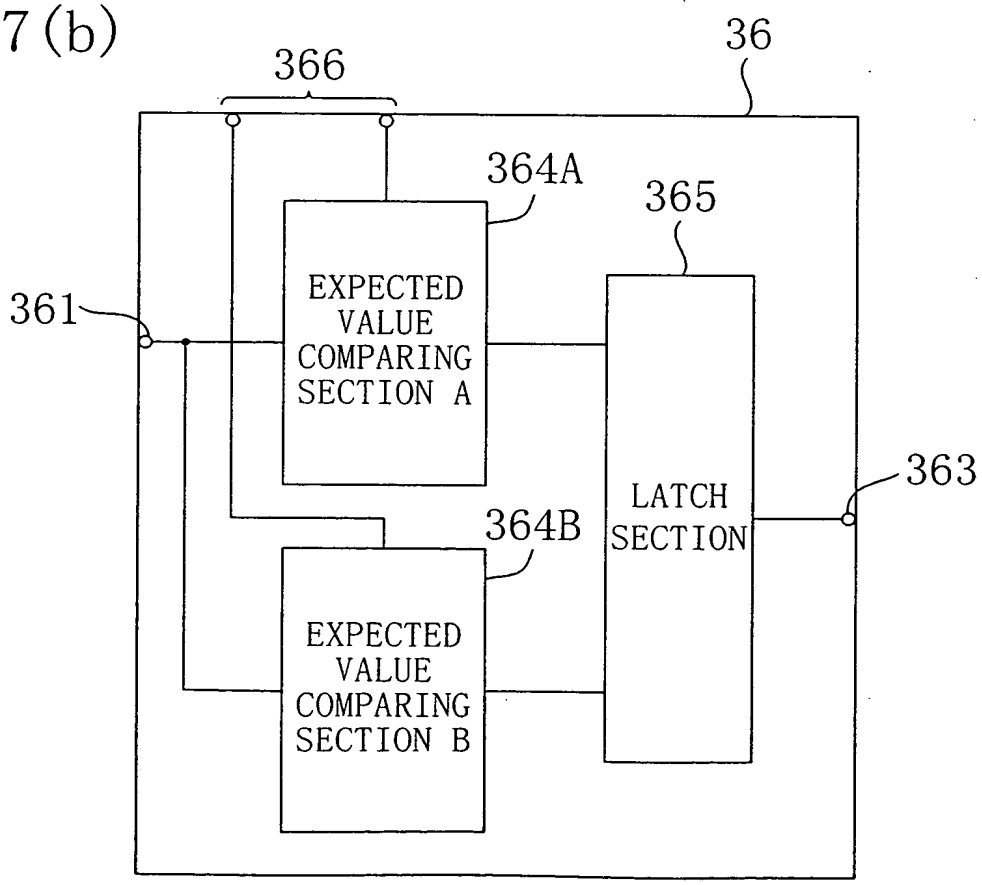

Fig. 18

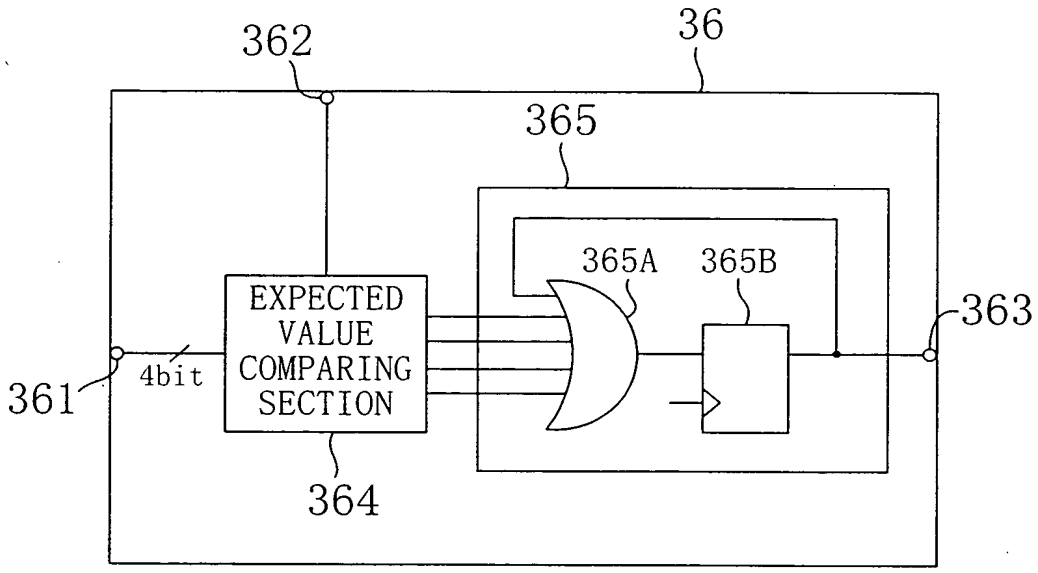
362
36
365
365A
365B
363
EXPECTED VALUE COMPARING SECTION
4bit
361
364

Fig. 19

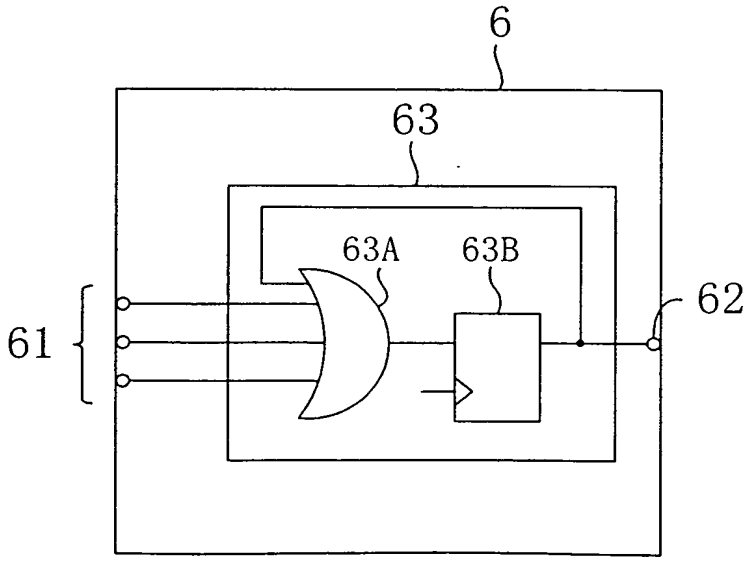
6
63
63A
63B
62
61

Fig. 20

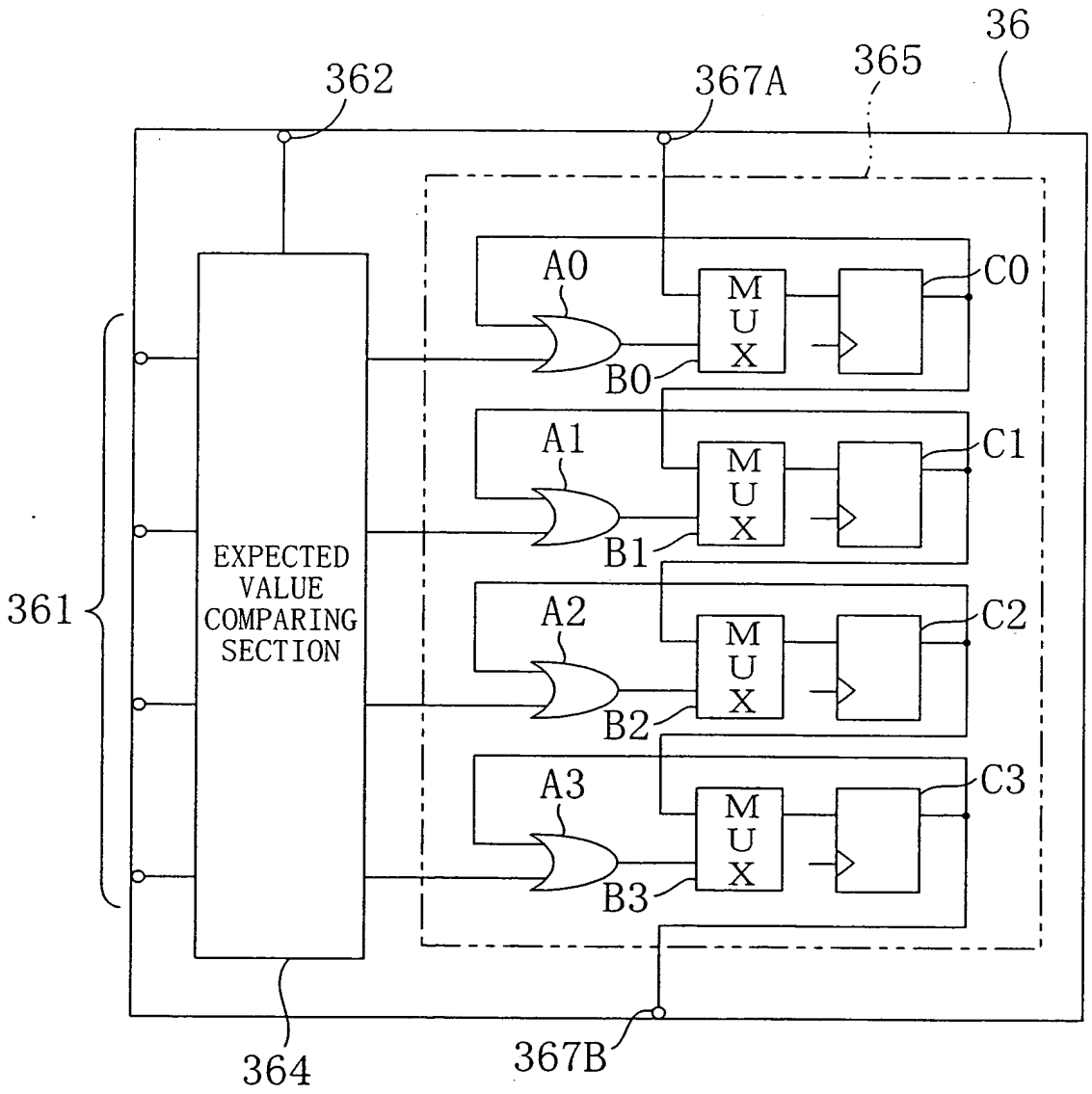
36
362
367A
365
A0
B0
C0
A1
B1
C1
A2
B2
C2
A3
B3
C3
MUX
EXPECTED VALUE COMPARING SECTION
361
364
367B

Fig. 21

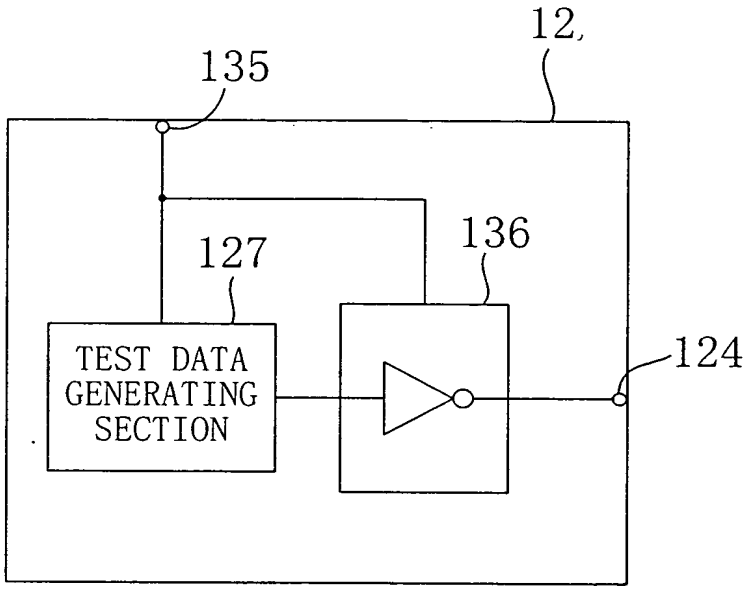

Fig. 22

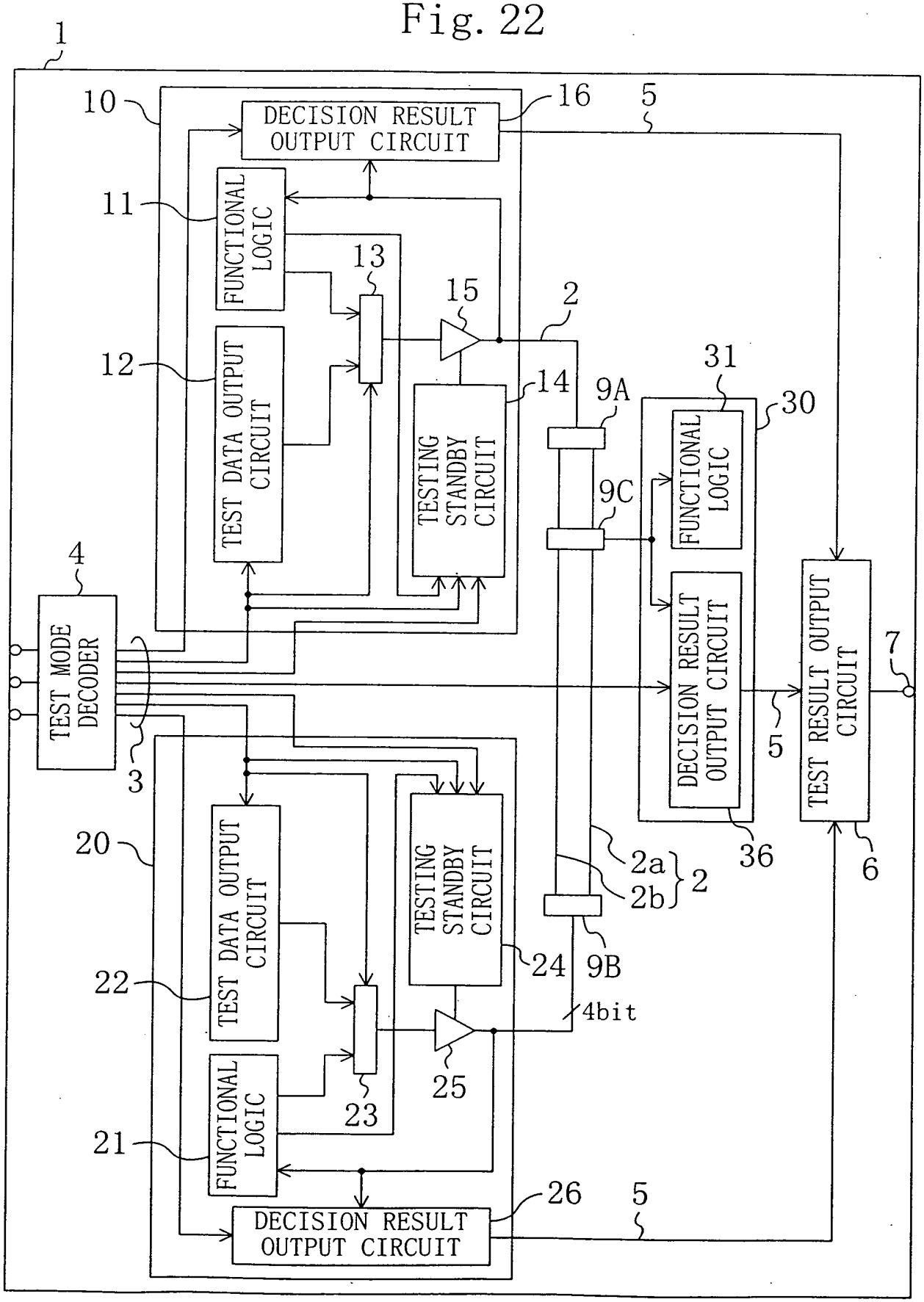
1
10
DECISION RESULT OUTPUT CIRCUIT
16
5
11
FUNCTIONAL LOGIC
13
15
2
12
TEST DATA OUTPUT CIRCUIT
14
TESTING STANDBY CIRCUIT
9A
31
30
FUNCTIONAL LOGIC
9C
4
TEST MODE DECODER
DECISION RESULT OUTPUT CIRCUIT
TEST RESULT OUTPUT CIRCUIT
7
5
3
20
TEST DATA OUTPUT CIRCUIT
TESTING STANDBY CIRCUIT
2a
2b
2
36
6
22
24
9B
4bit
25
23
21
FUNCTIONAL LOGIC
26
DECISION RESULT OUTPUT CIRCUIT
5

Fig. 23

TIME / TEST DATA	t 1	t 2
BIT 0	1	0
BIT 1	1	0
BIT 2	1	0
BIT 3	1	0
PATH CONTROL	1	1

Fig. 24

TIME / TEST DATA	t 1	t 2
BIT 0	1	0
BIT 1	1	0
BIT 2	1	0
BIT 3	1	0
PATH CONTROL	0	0

Fig. 25
Prior Art

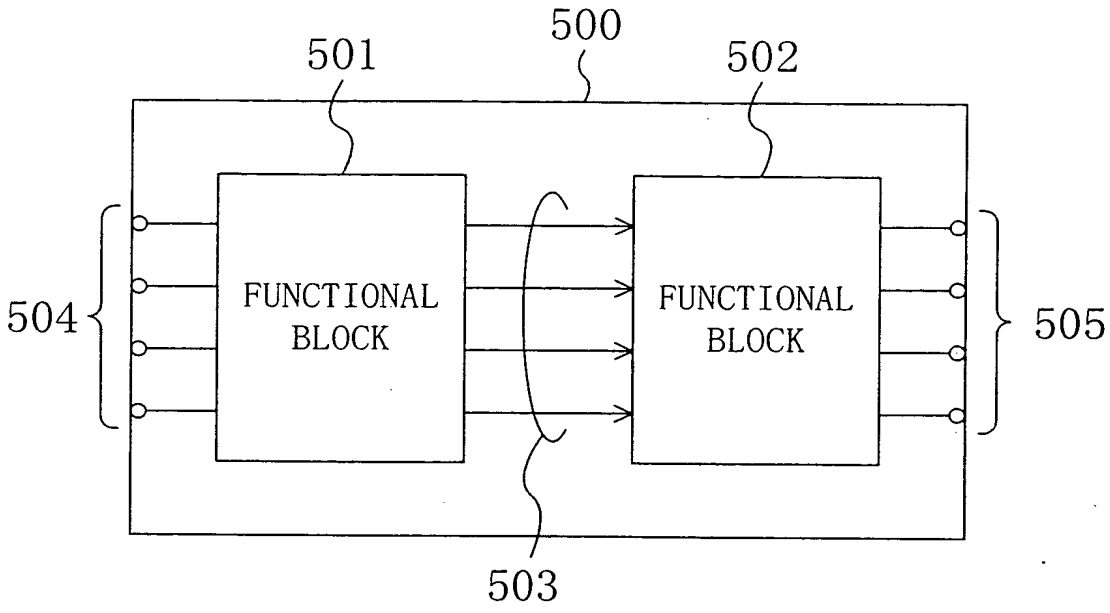

Fig. 26
Prior Art